Description

Process for the multi-stage production of diffusion-brazed joins for power components with semiconductor chips

The invention relates to a process for the multi-stage production of diffusion-brazed joins for power components with semiconductor chips, and to a power electronic component.

Diffusion-brazed joins are known from document DE 195 32 250 A1 and are used to produce a thermally stable join by means of diffusion-brazing. For this purpose, a first body is coated with a high-melting metal and a second body is coated with a low-melting metal. Then, the two bodies can be joined by a diffusion-brazed join at a predetermined temperature and under a predetermined contact pressure. In a diffusion-brazed join, high-melting intermetallic phases are formed, the melting points of which are higher than the melting point of the low-melting metal. The known process can be used to produce individual thermally stable joins in a power electronic component.

However, a power electronic component has a plurality of joins, which have to be realized in multi-stage processes. This produces unreliable joins.

It is an object of the invention to provide a process which allows the reliable production of thermally stable electronic components which are suitable for extreme thermal stresses. In particular, it is an object of the invention to provide a power electronic component which can withstand corresponding stresses.

The object is achieved by the subject matter of the independent claims. Advantageous refinements of the

invention will emerge from the dependent claims.

The invention provides a process for the multi-stage production of diffusion-brazed joins on a carrier underside and carrier top side to a substrate for the carrier underside and a further substrate for the carrier top side. In particular, the invention provides a multi-stage process for joining a semiconductor chip rear side to a chip island of a substrate and a semiconductor chip top side to conduction structures of a further substrate for power electronic components by diffusion brazing. For this purpose, the process includes the following process steps.

First of all, a first side of a carrier or semiconductor is coated with a first diffusion-brazing alloy. A diffusion-brazing alloy of this type includes a mixture of a high-melting metal component and a low-melting metal component, without intermetallic phases already having formed. Then, a second side of the carrier or semiconductor is coated with a second diffusion-brazing alloy. The first and second diffusion-brazing alloys belong to different diffusion-brazing systems in terms of their composition and metallic elements.

The first and second diffusion-brazing alloys are matched to one another by selection of materials and components in such a manner that the melting points of the diffusion-brazing alloys and of the diffusion-brazed joins are staggered in such a manner that a first melting point of the first diffusion-brazing alloy is lower than a second melting point of the second diffusion-brazing alloy, and that the second melting point is lower than a third melting point of a first diffusion-brazed join of the first diffusion-brazing alloy.

After the carrier has been coated on both sides, namely with the first and second diffusion-brazing alloys, first of all a first substrate is diffusion-brazed to the first side of the carrier or semiconductor by heating the first diffusion-brazing alloy to the first melting point. This forms a first thermally stable diffusion-brazed join, the melting point of which is higher than the second melting point of the second diffusion-brazing alloy. This is followed by a second substrate being diffusion-brazed to the second side of the carrier or semiconductor by heating the second diffusion-brazing alloy to the second melting point. Since this second melting point is lower than the third melting point of the first diffusion-brazed join, the existing first diffusion-brazed join is retained in a thermally stable manner during this multi-stage production with staggered melting points of the diffusion-brazing operations.

This process for the multi-stage production of diffusion-brazed joins has the advantage that both a diffusion-brazed join to the underside and a diffusion-brazed join to the top side of a carrier are possible, on account of the suitable matching of the diffusion-brazing systems for the underside and top side of the carrier. A power electronic component which is produced in this way does not have any weak points in the joining technology and can therefore be subjected to extremely high thermal stresses.

In this context, the invention takes account of the fact that a power electronic component with semiconductor chips has a substrate onto which semiconductor chips are brazed. Subsequent brazing of flat conductors to the top side of the semiconductor chips would lead to the brazed rear side becoming detached, which restricts the ability of the power component to withstand thermal stresses. Therefore, the

connections on the top side are often not produced by brazing, but rather by bonded joins between electrodes on the top side of the semiconductor chips and flat conductors which lead outward. Both conventional soldered joins and diffusion-brazed joins of the chip rear side to a substrate do not reduce the limited ability of bonded joins on the top side of power semiconductor chips to withstand thermal stresses. The invention increases the ability of power electronic components to withstand thermal stresses by producing thermally stable joins both on the rear side of the semiconductor chip and on the top side of the semiconductor chip.

Table 1 shows possible alloying partners for diffusion-brazed joins as well as the melting points which it is possible to use prior to formation of intermetallic phases as first and second melting points and the melting points of the intermetallic phases which are formed in a diffusion-brazed join, which should be taken into account as the third melting point when employing the process according to the invention. This table reveals preferred systems for the alloy composition of a first diffusion-brazing alloy and a second diffusion-brazing alloy.

A first diffusion-brazing alloy, which has a first melting point and a composition comprising Ga-yNi where 1% by weight < y < 20% by weight or Ga-xCu where 1% by weight < x < 40% by weight or Ga-yAg where 1% by weight < y < 40% by weight, can be applied to the first side of a carrier or a semiconductor chip. A second diffusion alloy, which includes In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight, can be applied to the second side. This staggering of the diffusion-brazing systems has the advantage that the first diffusion-brazing alloy has extremely low melting points between 26°C and 31°C,

and the two second diffusion-brazing alloys which are possible have relatively high first melting points of 144°C or 221°C. The last two diffusion-brazing systems listed in Table 1 cannot be used in combination with the first diffusion-brazing alloys indicated here, since their low melting points, at 280°C and 361°C, respectively, are already higher than some of the melting points of the intermetallic phases of the first diffusion-brazing alloy which form.

If the choice of low-melting first diffusion-brazing alloys is restricted further, it is possible to widen the options for higher-melting diffusion-brazing alloys to be used. For this purpose, a first diffusion-brazing alloy of the composition Ga-yNi where 1% by weight < y < 20% by weight or Ga-yAg where 1% by weight < y < 40% by weight is applied to the first side of a carrier or semiconductor chip. A second diffusion alloy of the composition In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, can be applied to the second side of a carrier or semiconductor chip. This staggering of the diffusion-brazing alloys has the advantage that even a melting point of 280°C is possible as the second melting point.

If the first diffusion-brazing alloy is restricted to just one diffusion-brazing system, for a brazing alloy with an extremely low first melting point of 26°C, it is possible to use a wide range of second diffusion alloys. For this purpose, the first side of a carrier or a semiconductor is coated with a diffusion alloy of the composition Ga-yAg where 1% by weight < y < 40% by weight. A second diffusion-brazing alloy of the composition In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight,

preferably where 10% by weight < x < 30% by weight or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

For applications in which a higher first melting point of over 100°C is desirable, the first side may have a first diffusion alloy of the composition In-xAg where 1% by weight < x < 30% by weight. Then, a second diffusion alloy of the composition Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is then applied to the second side.

A staggered diffusion system with a first and second diffusion alloy, in which the first diffusion alloy has a first melting point of over 200°C, is possible if the first side has a first diffusion alloy of the composition Sn-yAg where 1% by weight < y < 50% by weight. A second diffusion-brazing alloy of the composition Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

The highest demands imposed on melting points can be satisfied by staggering first and second diffusion-brazing alloys in such a way that a first diffusion-brazing alloy of the composition Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, is applied to the first side. A second diffusion-brazing alloy of the composition Au-yGe where 4% by weight < y < 50% by

weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

During heating to the brazing temperatures, relatively brittle intermetallic phases are formed; although these intermetallic phases do allow a thermally stable join to be produced, if there are differences in the expansion coefficient of the carrier or semiconductor chip and the substrates to be joined to it, there is a risk that the substrates will become detached from the carriers under thermal loads, on account of the brittle intermetallic phases, if the thermal stresses increase on account of the different expansion coefficients of the materials.

If, however, a layer of silver, copper or nickel is applied to each side of the carrier or of the semiconductor chip prior to the application of the diffusion-brazing alloys, this buffer layer has a damping action and advantageously reduces the stresses. This has the advantage that an interlayer of silver, copper or nickel or alloys thereof of this type forms a mechanical buffer, which enables a hard and brittle layer of intermetallic phases to be joined in a relatively soft and resilient manner to the carrier.

For diffusion-brazing alloys comprising Au-yGe where 4% by weight < y < 50% by weight, preferably 7% by weight < y < 20% by weight, it is advantageous to provide a buffer layer or interlayer of copper or a copper alloy, since intermetallic phases can then form between copper and germanium, with melting points of 614°C for Cu_3Ge and 742°C for Cu_5Ge.

Silver or copper layers as buffer layers may preferably also be used prior to the application of a diffusion-brazing alloy comprising Sn-yAg where 1% by weight < y

< 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight.

To avoid diffusion or alloying of the metal components of the alloys or buffer layers with a semiconductor chip material or a metalization material, such as aluminum for semiconductors, a layer sequence comprising a structured aluminum layer and a titanium layer deposited on top of it is applied prior to the application of a diffusion-brazing alloy to the sides of a semiconductor chip. The aluminum produces a low-resistance transition to the semiconductor material, and the titanium serves as a diffusion barrier to the various metal components of the diffusion-brazing alloys.

A further aspect of the invention provides a power electronic component with a semiconductor chip, the rear side of which is diffusion-brazed to a chip island. Flat conductors are diffusion-brazed to contact surfaces on the top side of the semiconductor chip. The brazed joins include different diffusion-brazing systems, with a first diffusion-brazing alloy on the rear side and a second diffusion-brazing alloy on the top side of the semiconductor chip. For this purpose, the first and second diffusion-brazing alloys have different melting points.

It is in this case possible to use the diffusion-brazing systems listed above. Each of the semiconductor chips of the power component has a layer sequence made up of aluminum and titanium directly on both its rear side and its top side, in order to avoid diffusion and reaction of the components of the alloy with the aluminum and the semiconductor material. A metal layer as buffer layer of copper or silver or nickel or alloys thereof may be arranged on the sides between this layer

sequence and the diffusion-brazing alloys, in order on the one hand to promote the formation of a diffusion-brazed join and on the other hand to allow a mechanical buffer for the different expansion properties of semiconductor chips and substrates.

To summarize, it can be stated that a high-melting join comprising intermetallic compounds, the melting point of which following the joining operation is higher than the subsequent process temperatures, can be formed by using suitable alloy metalizations on a semiconductor chip. To enable a semiconductor chip rear side to be joined to the corresponding substrate first, and then a semiconductor chip top side to be joined to the corresponding substrate, two different alloy systems, which are suitable on account of their melting and joining properties, are used.

For example, for hot-joining of a first chip side by means of Au-Sn (T_{melt} = 280°C), it is possible to form a high-melting metallurgical contact comprising intermetallic phases with the first substrate. A silver layer is used firstly as a reaction partner for Au-Sn and secondly as a mechanically soft buffer to compensate for any differences in the expansion coefficients between substrate and semiconductor chip. In this case, at a first temperature of 280°C, the alloy on the second chip surface, which has a diffusion-brazing alloy comprising Au-Ge (T_{melt} = 361°C), should not melt and the reaction of the corresponding intermetallic phases of this second diffusion-brazing alloy should not be started.

In this context, minimal solid-state diffusion can be ignored. In a second diffusion-brazing step, the chip, which has already been joined to the first substrate, can then again be introduced into a hot process, in which the other, second side of the semiconductor chip

surfaces is then joined to the second substrate. The second metalization system or diffusion-brazing system includes Au-Ge, and the buffer used in this case is a copper layer, which simultaneously serves as a reaction layer. Since the first diffusion-brazing alloy is already fully alloyed, it will no longer melt, especially since the diffusion-brazing temperatures of the intermetallic phases of the first diffusion-brazing system have a melting point > 400°C.

The use of two diffusion brazing solders as metalizations on the top side and rear side of a semiconductor chip with two different melting points can allow staged joining firstly of one side and then of the other side without the second diffusion brazing solder melting during the first joining step, so that it reacts and can become unusable. On account of the use of different diffusion brazing solders, the present invention only allows a second joining process at a high temperature, since when joining by the formation of an alloy, the melting point of the first join increases so as to be higher than the melting point of the second join.

If appropriate, a “diffusion-brazing alloy” is also to be understood as meaning a diffusion-brazing mixture. This applies in particular if no intermetallic phases have yet been produced. In a preliminary state of this type, the fractions of the subsequent alloy are already present as components. When it uses the term “diffusion-brazed join”, the invention relates to the states of the later alloy with intermetallic phases in the microstructure.

The invention will now be explained in more detail with reference to the appended figures, in which:

figure 1 shows a diagrammatic cross section through a

carrier with diffusion-brazed joins to a lower first substrate and to an upper second substrate in accordance with one embodiment of the invention,

figure 2 shows a diagrammatic cross section through a carrier which has a first diffusion-brazing alloy on its underside and a second diffusion-brazing alloy on its top side, before the carrier is diffusion-brazed to a first substrate,

figure 3 shows a diagrammatic cross section through the carrier shown in figure 2 following first diffusion-brazing of the carrier to the substrate,

figure 4 shows a diagrammatic cross section through the carrier shown in figure 3 prior to the application of a second substrate to the top side of the carrier,

figure 5 shows a diagrammatic cross section through the carrier shown in figure 4 following diffusion-brazing of the second substrate to the top side of the carrier.

Figure 1 shows a diagrammatic cross section through a carrier 12 made from a semiconductor chip material with diffusion-brazed joins 16 to a lower first substrate 4 and an upper second substrate 5 in accordance with one embodiment of the invention. On its underside 2, the carrier 12 has an aluminum coating 20 which is covered by a titanium layer 21. This layer sequence 19 protects the aluminum and the semiconductor material of the carrier 12 from the components of the diffusion-brazing systems. In this case, the titanium layer forms a diffusion barrier and therefore also protects the

aluminum layer.

The diffusion-brazed joins 16, 17 are matched to one another in such a manner that first of all the diffusion-brazed join 16 can be produced at a low, first melting point, forming intermetallic phases, so that the second diffusion-brazed join 17 can be realized at a significantly higher, second melting point. The first diffusion-brazed join 16 in practice joins the rear side of a semiconductor chip 13 to a substrate 8, which is designed, for example, as a chip island 7, with a buffer layer 18 of copper or silver or alloys thereof being arranged as buffer and compensation layer between the diffusion-brazed join 16 and the semiconductor 13. This buffer layer 18, if it includes silver, is at the same time a reservoir of silver for forming the diffusion-brazed layer 16.

In a first embodiment of the invention, the diffusion-brazed layer 16 is formed from a diffusion-brazing alloy which comprises Au-xSn where 10% by weight < x < 30% by weight. The buffer layer 18 is composed of silver. The high thermal stability of this diffusion-brazed layer 16 is based on intermetallic phases between silver and tin, namely Ag_3Sn, with a melting point of 480°C, and Ag_5Sn, with a melting point of 724°C. These melting points of the intermetallic compounds are significantly higher than a second melting point which is required for the formation of the second diffusion-brazed layer 17. This second diffusion-brazed layer 17 is arranged on the top side 3 of the carrier 12.

On account of the semiconductor chip material used in this embodiment of the invention, the top side 9 of the semiconductor 13 is initially covered by the layer sequence 19 comprising an aluminum layer 20 and a titanium layer 21. This is followed by a buffer layer

18 comprising copper. The diffusion-brazed layer 17, which is joined to a second substrate 5 in such a manner as to withstand high temperatures, is arranged on this buffer layer 18.

The high thermal stability of the second diffusion-brazed layer 17 is achieved by intermetallic phases comprising copper and germanium. In this case, the intermetallic phase Cu_3Ge has a melting point of 614°C, and the intermetallic phase Cu_5Ge has a melting point of 743°C. In this embodiment of the invention, the second substrate is a flat conductor structure which is joined to contact surfaces of the semiconductor 13 by means of a diffusion-brazing process.

The overall structure as revealed in figure 1 represents a diagrammatic cross section through a power electronic component 11, which is both mechanically and thermally optimized on account of the diffusion-brazed joins 16 and 17 and the buffer layers 18. In this context, the buffer layer 18 ensures that thermal stresses between the substrates and the carrier are compensated for, and the diffusion-brazed layers 16 and 17 ensure that a thermally stable join to the substrates is maintained even at high operating temperatures of a power electronic component.

Figures 2 to 4 show the production of diffusion-brazed joins on a carrier 12, as shown in figure 1, in stages.

A first stage of this production process is shown in figure 2, which shows a diagrammatic cross section through a carrier 12, which has a first diffusion-brazing alloy 14 on its underside 2 and a second diffusion-brazing alloy 15 on its top side 6. A buffer layer 18, which is composed of silver or copper on the underside of the carrier and has a copper layer on the top side of the carrier, is arranged between the

diffusion-brazing alloys 14 and 15 and the carrier 12. Furthermore, to protect the semiconductor material of the carrier 12, a layer sequence comprising aluminum and titanium has been applied to the sides, the aluminum producing good contact with the semiconductor material and the titanium serving as a diffusion barrier for the material of the buffer layers, so that they do not react either with the aluminum or with the semiconductor material. A carrier 12 which has been prepared in this manner can then be placed onto a first substrate 4 and joined by way of the underside 2 of the carrier 12 in a diffusion-brazing process.

Figure 3 shows a diagrammatic cross section through the carrier 12 shown in figure 2 after first diffusion-brazing of the carrier 12 onto the first substrate 4 or 8 at a melting point of over 280°C. This melting point 280°C is required since the diffusion-brazing alloy 14 includes Au-xSn where 10% by weight < x < 30% by weight. The intermetallic phases formed at this first melting point of 280°C include Ag_3Sn with a melting point of 480°C and Ag_5Sn with a melting point of 724°C. On account of the high first melting point of 280°C, the time required for the diffusion-brazing is significantly shorter than when using diffusion-brazing alloys with low first melting points of less than 50°C.

When intermetallic phases are being formed in the diffusion-brazed join 16, some of the buffer layer 1 of silver can be consumed as a reaction partner for the intermetallic phases, which is represented in figure 3 by a reduced thickness of the buffer layer 18 compared to the buffer layer 18 shown in figure 2.

Figure 4 shows a diagrammatic cross section through the carrier 12 shown in figure 3 prior to the application of a second substrate 5 or 10 to the top side 3 of the carrier 12. This second substrate may comprise flat

conductors which are to be applied to contact surfaces of a semiconductor chip top side. The carrier 12 therefore includes a semiconductor material, which is initially provided with a low contact resistance to the semiconductor chip material by means of an aluminum layer 20, and then a diffusion-inhibiting titanium layer 21 is arranged on the aluminum layer 20. This layer sequence 19 is followed by a buffer layer 18, which on the top side 3 of the carrier 12 consists of copper. This copper is matched to the diffusion-brazing alloy 15 comprising Au-yGe where 7% by weight < y < 20% by weight, remainder Au, so that intermetallic phases of copper and germanium are formed at the second melting point of over 361°C. The melting point of the intermetallic phases comprising Cu_3Ge and Cu_5Ge are 614°C and 743°C, respectively. Prior to diffusion-brazing, the second substrate 5 is pressed onto the second diffusion-brazing alloy 15, and a diffusion-brazed join, as shown in figure 5, is formed at the corresponding brazing temperature of over 361°C.

Figure 5 shows a diagrammatic cross section through the carrier 12 shown in figure 4 after diffusion brazing of the second substrate 5 onto the top side 3 of the carrier 12 has taken place. This high melting point of over 361°C allows rapid diffusion brazing without the diffusion brazing 16 on the underside of the carrier 12 being damaged, especially since the melting points of the intermetallic phases which have formed there are greater than 400°C.